What is claimed is:

1. An apparatus, comprising:

- a low voltage swing (LVS) circuit having a plurality of alternating LVS pre-charging and evaluation phases;

- a clock generator for generating at least one clock signal; and

- a select logic circuit coupled to the LVS circuit and the clock generator and responsive to the clock signal and a plurality of input data signals to generate a plurality of select signals for the LVS circuit, each of the select signals occurring during one of the LVS evaluation phases and having a turning-on edge triggered by one of the input data signals and a turning-off edge triggered by the clock signal independently of the input data signals.

2. The apparatus according to claim 1, wherein the clock generator is operable to generate a master clock signal, a domino clock signal and a slave clock signal; and wherein the select logic circuit further includes at least one master latch coupled to the clock generator and responsive to one of the input data signals and the master clock signal to generate a latch output signal; at least one D1-domino coupled to the clock generator and the master latch to generate a domino output signal in response to the latch output signal and the domino clock signal; and at least one slave latch coupled to the clock generator and the D1-domino to generate one of the select signals in response to the domino output signal and the slave clock signal.

3. The apparatus according to claim 2, wherein the slave latch is a set dominant latch and the turning-off edge is triggered in response to the slave clock signal.

4. The apparatus according to claim 3, wherein the D1-domino and the slave latch are disposed in an in-phase relationship and the master latch and slave latch are disposed in an out-of-phase relationship.

5. The apparatus according to claim 4, wherein the select logic circuit further comprises at least one pair of buffering inverters coupled between the slave latch and the LVS circuit.

6. The apparatus according to claim 2, wherein the slave clock signal and the domino clock signal are the same and wherein the turning-off edge of each of the select signals has a one-gate delay through the slave latch and the turning-on edge of each of the select signals has a two gate delay through the D1-domino and the slave latch.

7. The apparatus according to claim 2, wherein the clock generator is operable to speed up the slave clock signal relative to the master clock signal and the master clock signal and the domino clock signal are the same.

8. The apparatus according to claim 2, wherein the clock generator includes a clock source to generate the master clock and the slave clock signal with a clock advance relative to the master clock and further includes a delay buffer coupled to the clock source and a gate of the D1-domino to provide the domino clock signal in response to the slave clock signal, with the delay buffer having a clock delay to substantially cancel the clock advance.

9. The apparatus according to claim 2, wherein the LVS circuit has a plurality of input terminals; and the select logic circuit includes a plurality of master latches with each master latch coupled to the clock generator and capable of receiving one of the input data signals; a plurality of D1-dominos with each of the D1-dominos coupled to one of the master latches and the clock generator; and a plurality of slave latches with each of the slave latches coupled to one of the D1-dominos and the clock generator.

10. The apparatus according to claim 2, wherein the select logic circuit further includes a plurality of pairs of the buffering inverters with each of the pairs being coupled between one of the slave latches and to one of the input terminals of the LVS circuit.

11. The apparatus according to claim 2, wherein the D1-domino has a plurality of alternating domino pre-charging and evaluation phases; the D1-domino is capable of generating the domino output signal during one of the domino evaluation phases; and the slave latch is capable of generating the select signal during one of the LVS evaluation phases.

12. An apparatus, comprising:

- a low voltage swing (LVS) circuit;

- a clock generator to generate a master, a domino, and a slave clock signal;

- a select logic circuit further including a plurality of master latches with each of the master latches being coupled to the clock generator and responsive to one of a plurality of input data signals and the master clock signal to generate one of a plurality of latch output signals; a plurality of D1-dominos with each of the D1-dominos being coupled to the clock generator and one of the master latches to generate one of a plurality of domino output signals in response to one of the latch output signals and the domino clock signal; and a plurality of slave latches with each of the slave latches being coupled to the clock generator and one of the D1-dominos to generate one of a plurality of select signals for the LVS circuit in response to the one of the domino output signals and the slave clock signal.

13. The apparatus according to claim 12, wherein the D1-dominos and the slave latches are disposed in an in-phase relationship and the master latches and slave latches are disposed in an out-of-phase relationship.

14. The apparatus according to claim 13, wherein each of the slave latches is a set dominant latch and a turning-off edge of each of the select signals is triggered in response to the slave clock signal and a turning-on edge of each of the select signals is triggered in response to one of the input data signals.

15. The apparatus according to claim 12, wherein the clock generator is operable to speed up the slave clock signal relative to the master clock signal and the master clock signal and the domino clock signal are the same.

16. The apparatus according to claim 12, wherein the clock generator includes a clock source to generate the master clock and the slave clock signal with a clock advance relative to the master clock and further includes a delay buffer coupled to the clock source and the D1-dominos to provide the domino clock signal in response to the slave clock signal, with the delay buffer having a clock delay to substantially cancel the clock advance.

17. The apparatus according to claim 12, wherein the LVS circuit has a plurality of input terminals, the select logic circuit further comprises a plurality of pairs of buffering inverters, with each of the pairs of buffer inverters being coupled between one of the slave latches and one of the input terminals of the LVS circuit.

18. The apparatus according to claim 12, wherein the second and domino clock signals are the same and wherein the turning-off edge of each of the select signals has a one-gate delay through one of the slave latches and the turning-on edge of each of the select signals has a two gate delay through one of the D1-dominos and one of the slave latches.

19. A system, comprising:

- an integrated circuit including

- a low voltage swing (LVS) circuit having a plurality of alternating LVS pre-charging and evaluation phases;

- a clock generator for generating at least one clock signal; and

- a select logic circuit coupled to the LVS circuit and the clock generator and responsive to the clock signal and a plurality of input data signals to generate a plurality of select signals for the LVS circuit, each of the select signals occurring during one of the LVS evaluation phases and having a turning-on edge triggered by one of the input data signals and a turning-off edge being triggered by the clock signal;

- a dynamic random access memory coupled to the integrated circuit; and

- an input/output interface coupled to the integrated circuit.

20. The system according to claim 19, the LVS circuit comprises a multiplexer LVS circuit.

21. The system according to claim 20, the integrated circuit further comprises a central processor unit including the multiplexer LVS and the select logic circuit.

22. The system according to claim 22, wherein the integrated circuit is a microprocessor.

23. The system according to claim 22, wherein the input/output interface comprises a networking interface.

24. The system according to claim 23, wherein the system is a selected one of a set-top box, an entertainment unit and a DVD player.

25. A method of generating a plurality of select signals for a low voltage swing (LVS) circuit having a plurality of alternating LVS pre-charging and evaluation phases, comprising:

- generating a plurality of select signals in response to a plurality of input data signals, each of the select signals occurring during one of the LVS evaluation phases and having a turning-on edge and a turning-off edge; and

- adjusting the turning-off edge of each of the select signals independently of the input data signals to increase a difference between an arrival time at the LVS circuit of the turning-off edge of each of the select signals and an arrival time at the LVS circuit of the turning-on time of a next one of the select signals.

26. The method according to claim 25, further comprising generating at least one clock signal and wherein the adjusting the turning-off edge includes triggering the turning-off edge based upon the clock signal.

27. The method according to claim 26, wherein adjusting the turning-off edge of each of the select signals includes providing a two gate delay first through a D1-domino and then through a slave latch for the turning-on edge of the select signal and providing a one gate delay through the slave latch for the turning-off edge of the select signal.

28. The method according to claim 27, wherein generating at least one clock signal includes generating a domino clock signal for the D1- domino and a slave clock signal for the slave latch and wherein adjusting the turning-off edge of each of the select signals further includes speeding up the turning-off edge of the select signal by advancing the slave clock signal relative to domino clock signal and triggering the turning-off edge based upon the slave clock signal.

29. The method according to claim 28, wherein adjusting the turning-off edge of each of the select signals includes passing the input data signals first through a master latch and then through the D1-domino and the slave latch; and operating the master latch and slave latch out-of-phase and the D1-domino and slave latch in-phase.

30. The method according to claim 29, wherein generating a plurality of select signals includes buffering the select signals prior to arriving at the LVS circuit by at least a pair of buffering inverters.